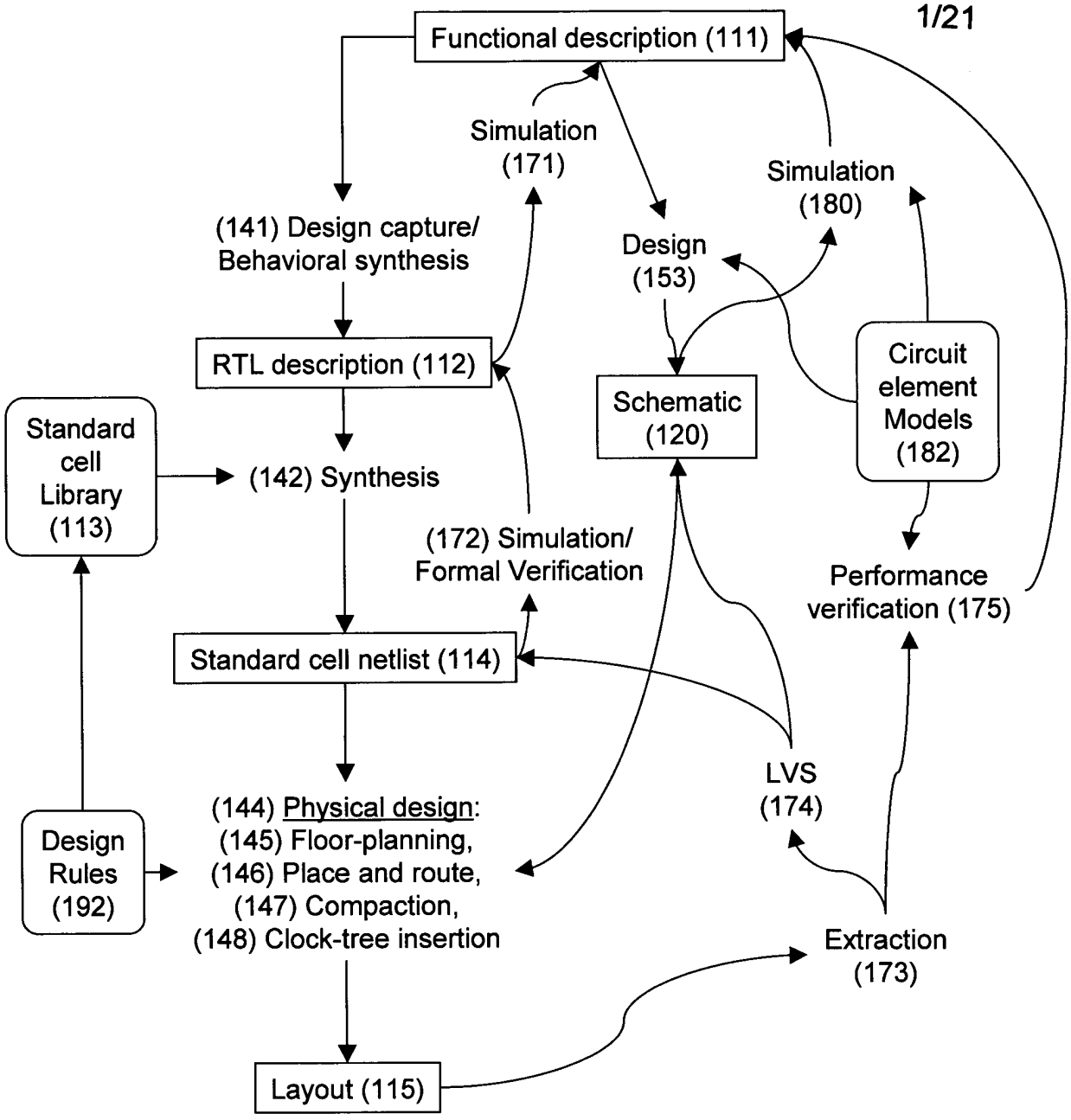
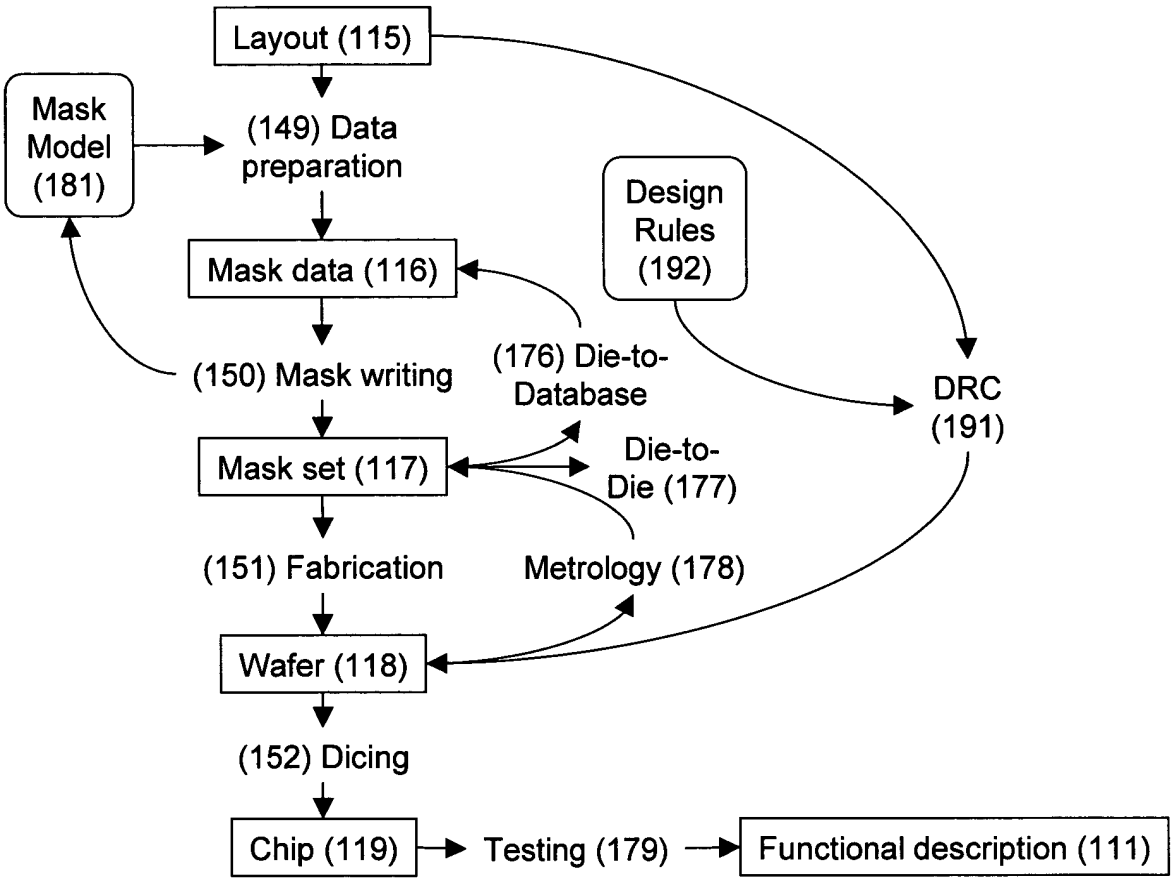


(a) Design aspect

Figure 1a (prior art)



(b) Manufacturing aspect

Figure 1b (prior art)

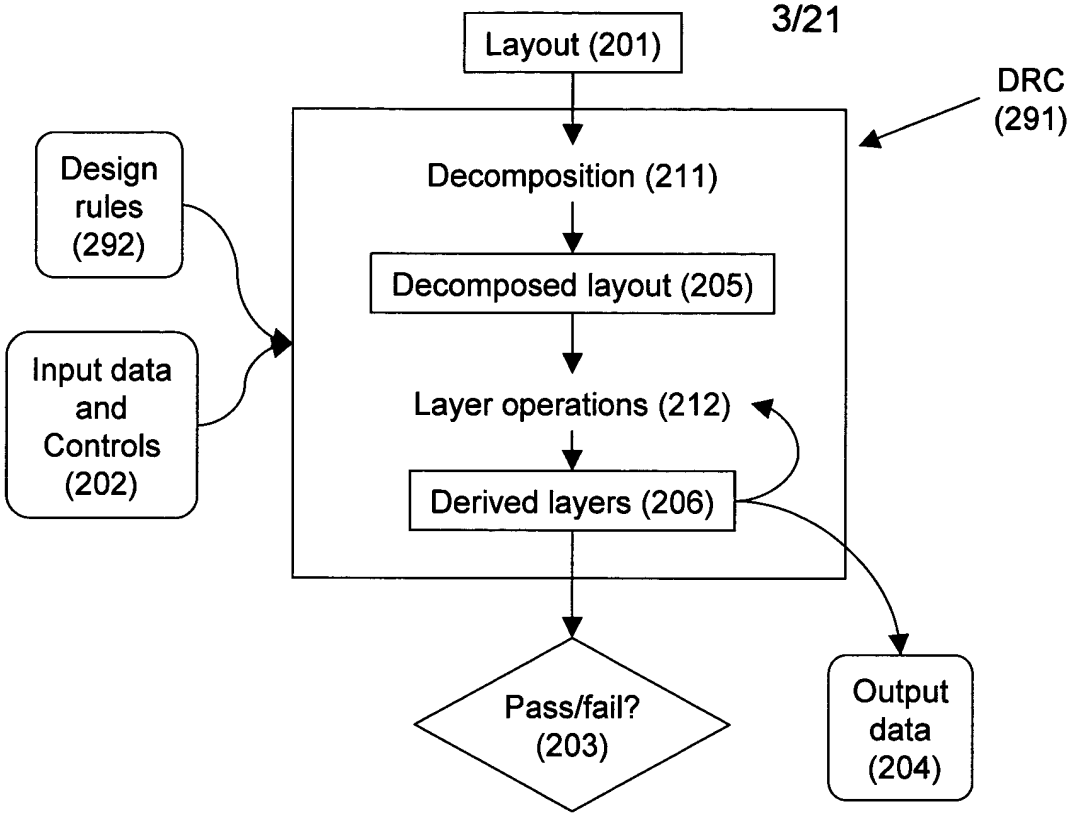


Figure 2 (prior art)

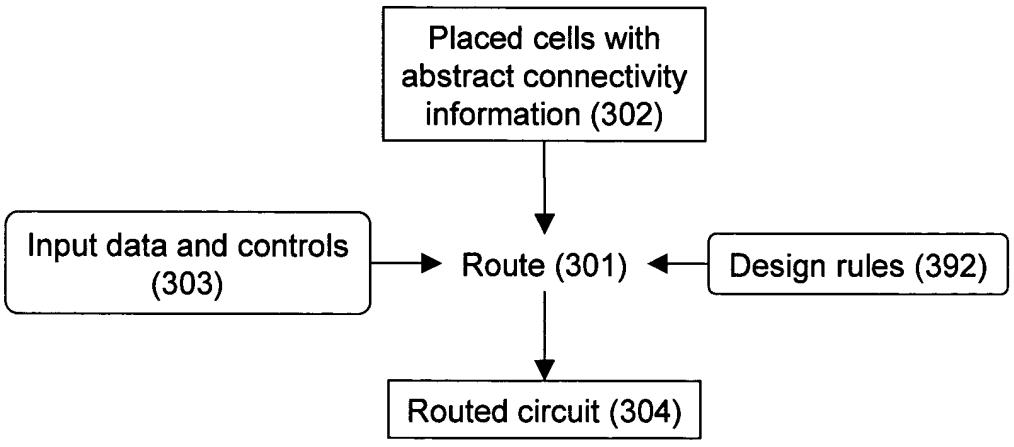

Placed cells with abstract connectivity information (302)
Input data and controls (303)
Route (301)
Design rules (392)
Routed circuit (304)

Figure 3 (prior art)

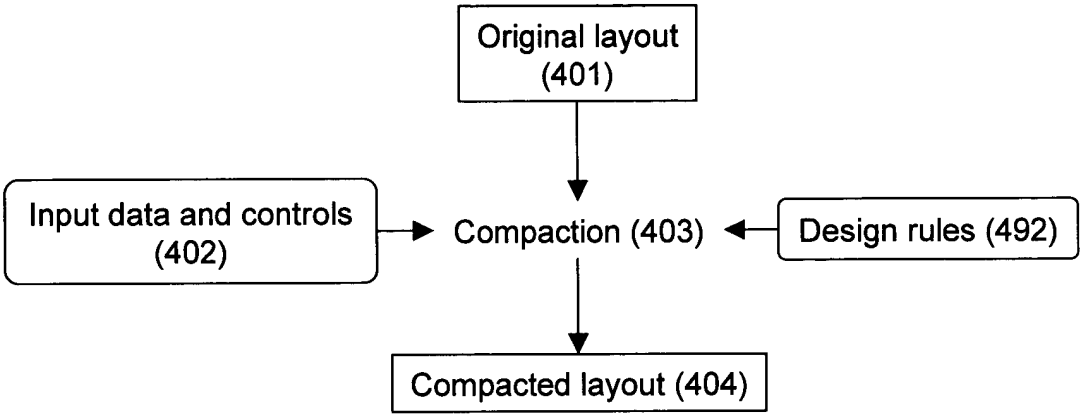


Figure 4 (prior art)

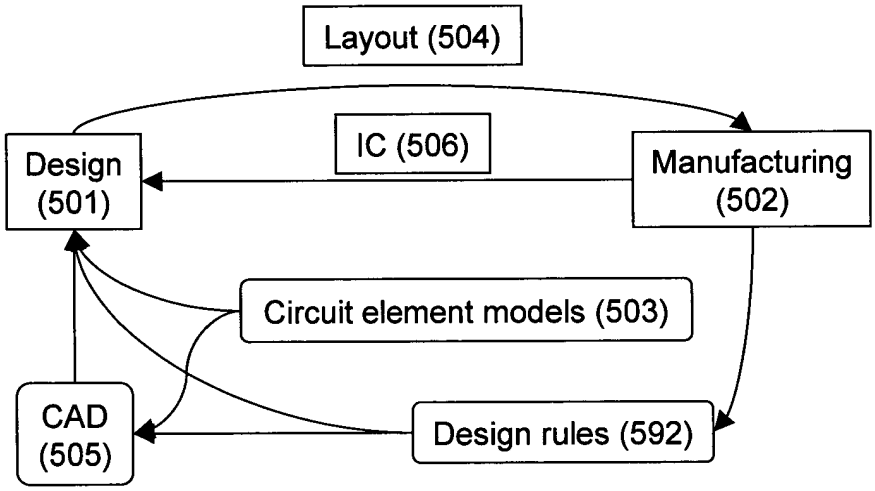


Figure 5 (prior art)

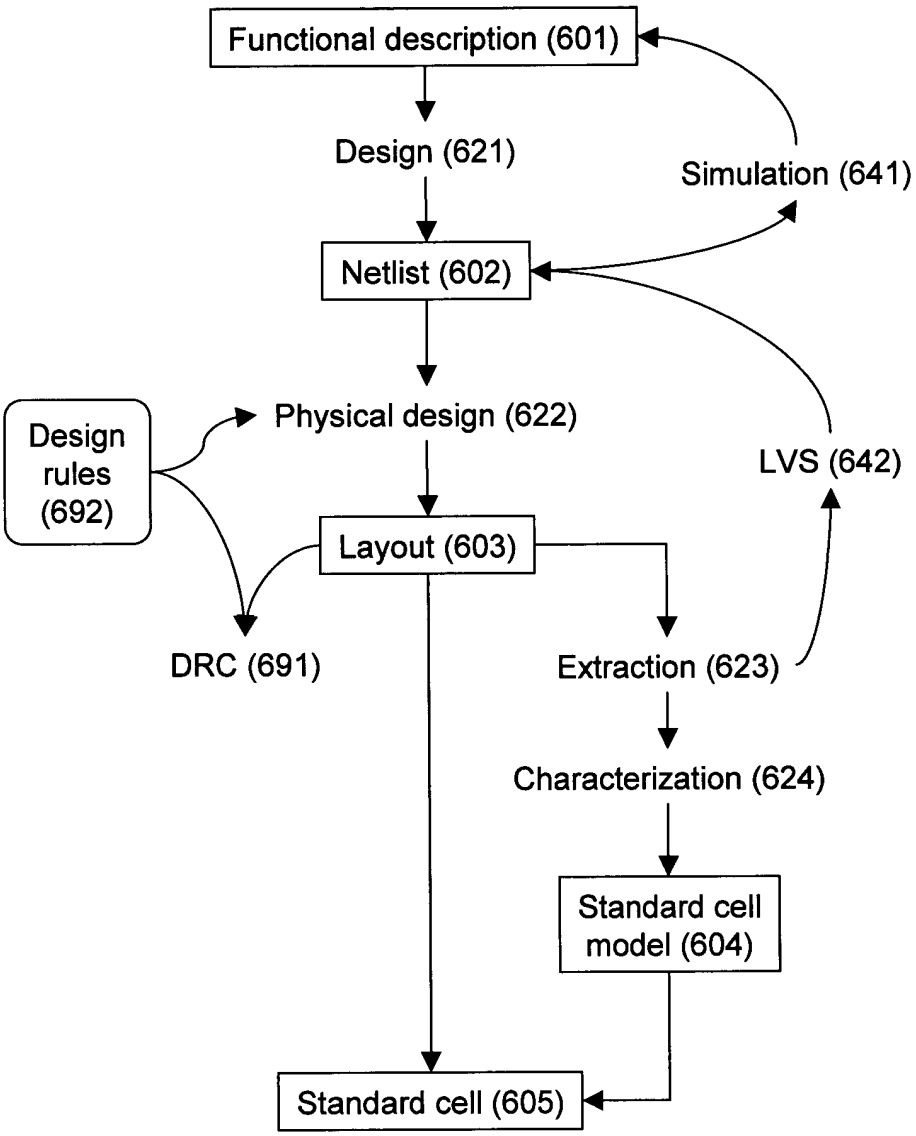


Figure 6 (prior art)

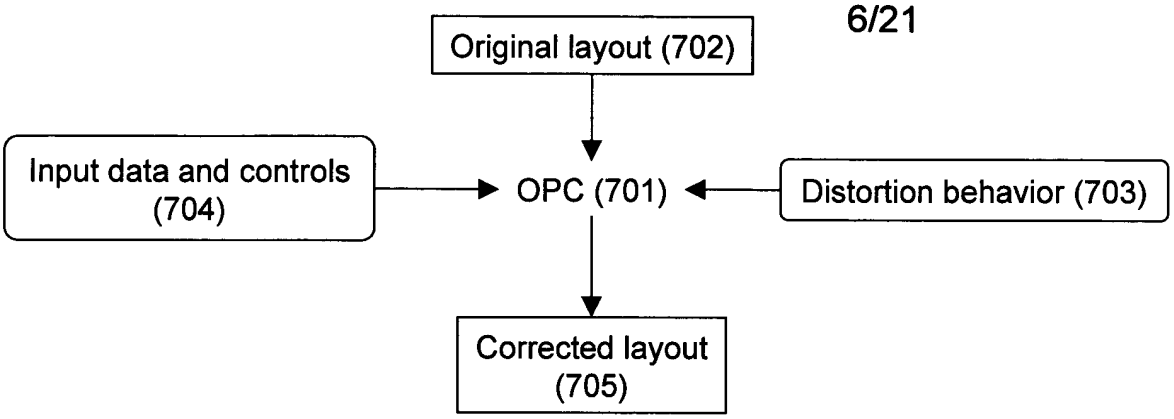


Figure 7 (prior art)

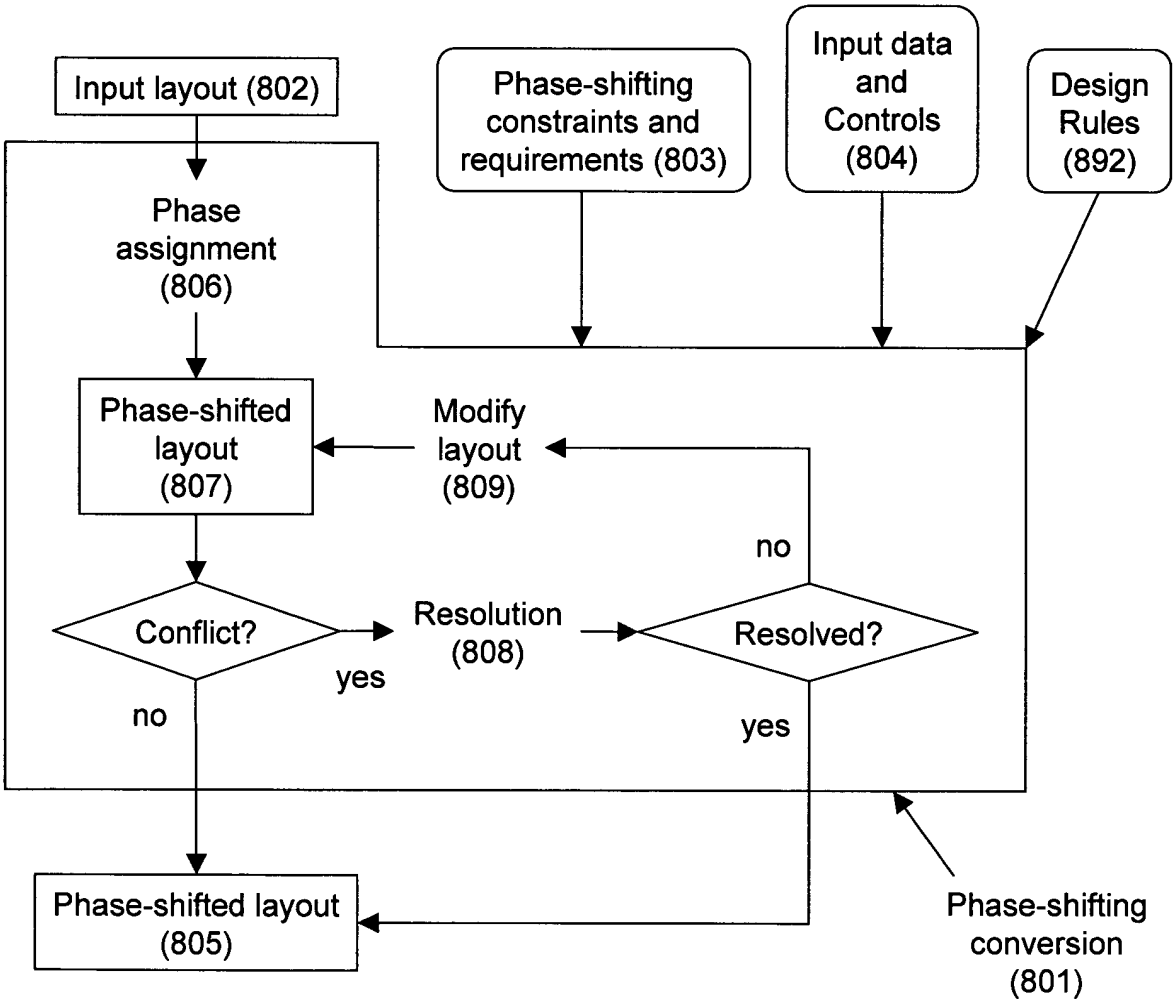


Figure 8 (prior art)

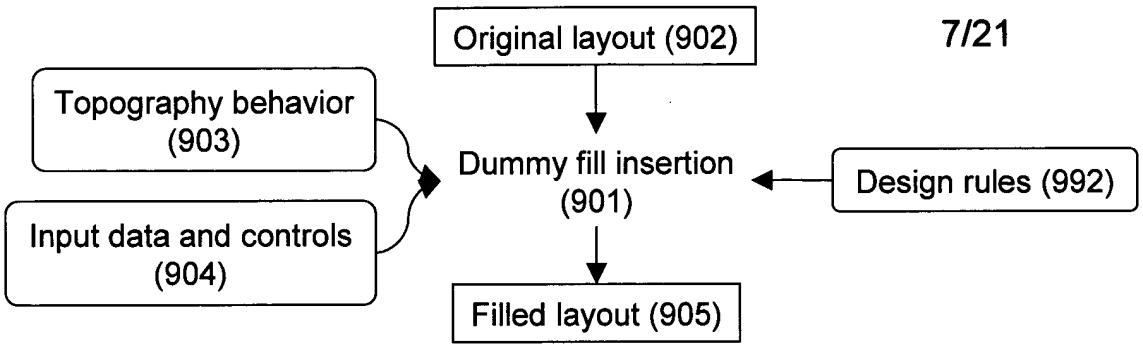


Figure 9 (prior art)

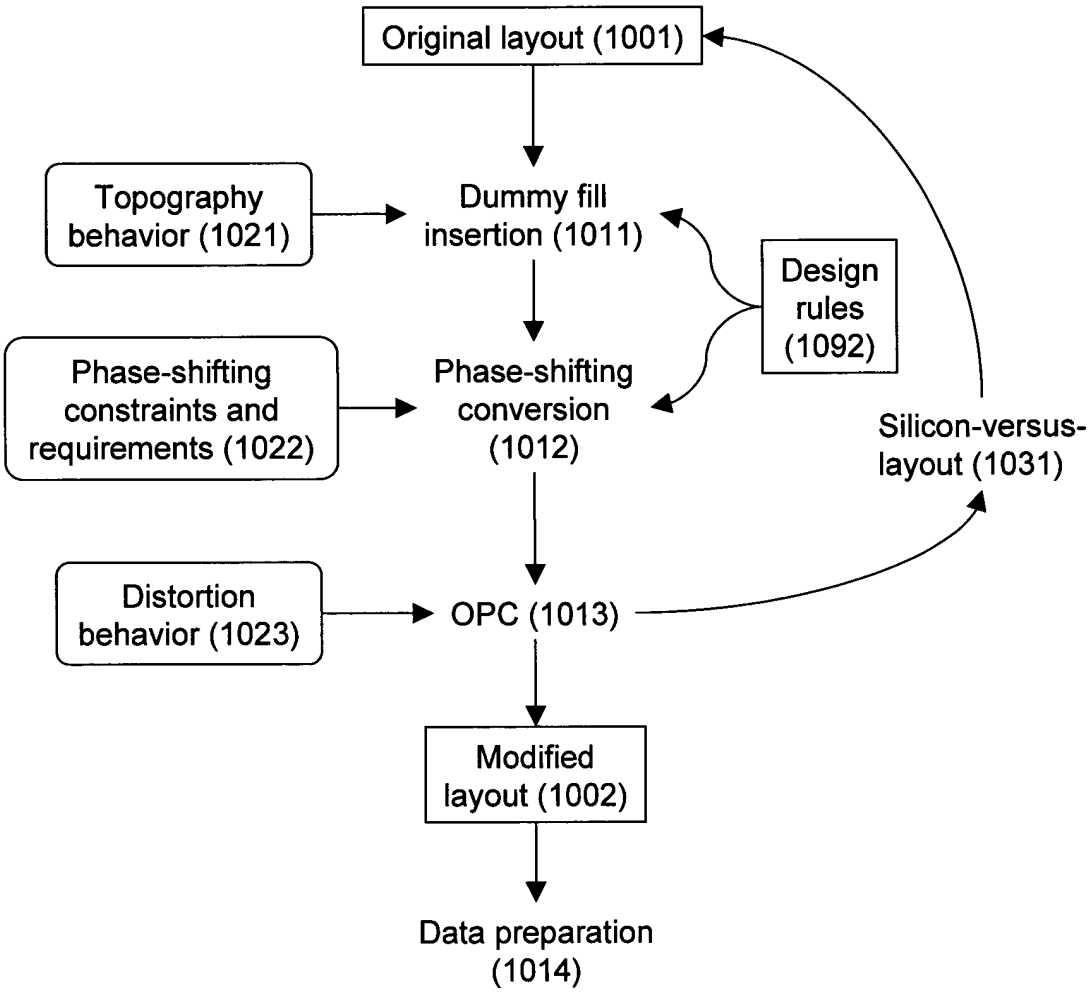


Figure 10 (prior art)

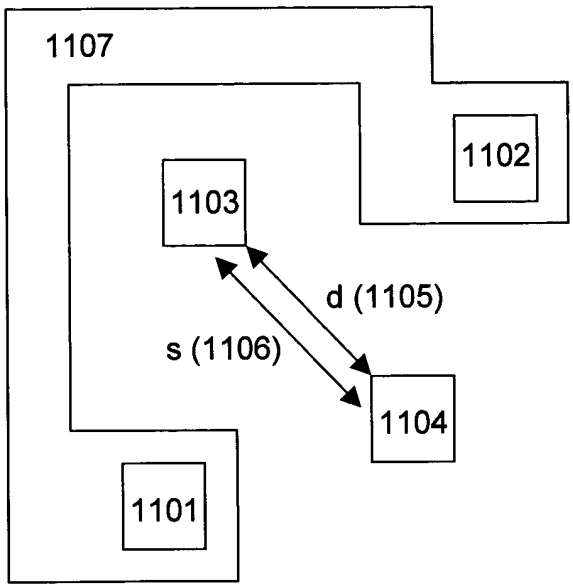


Figure 11a (prior art)

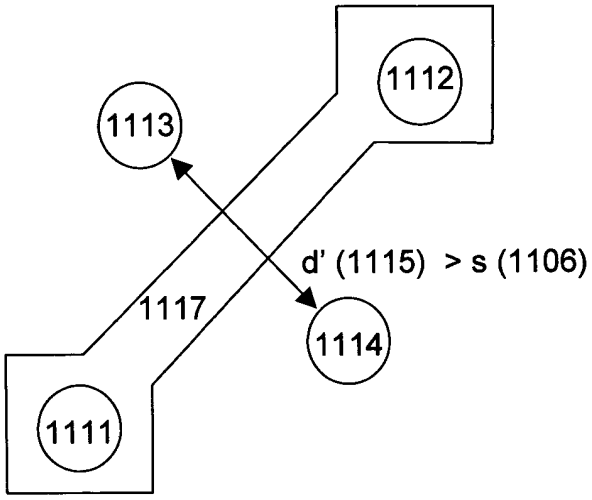


Figure 11b (prior art)

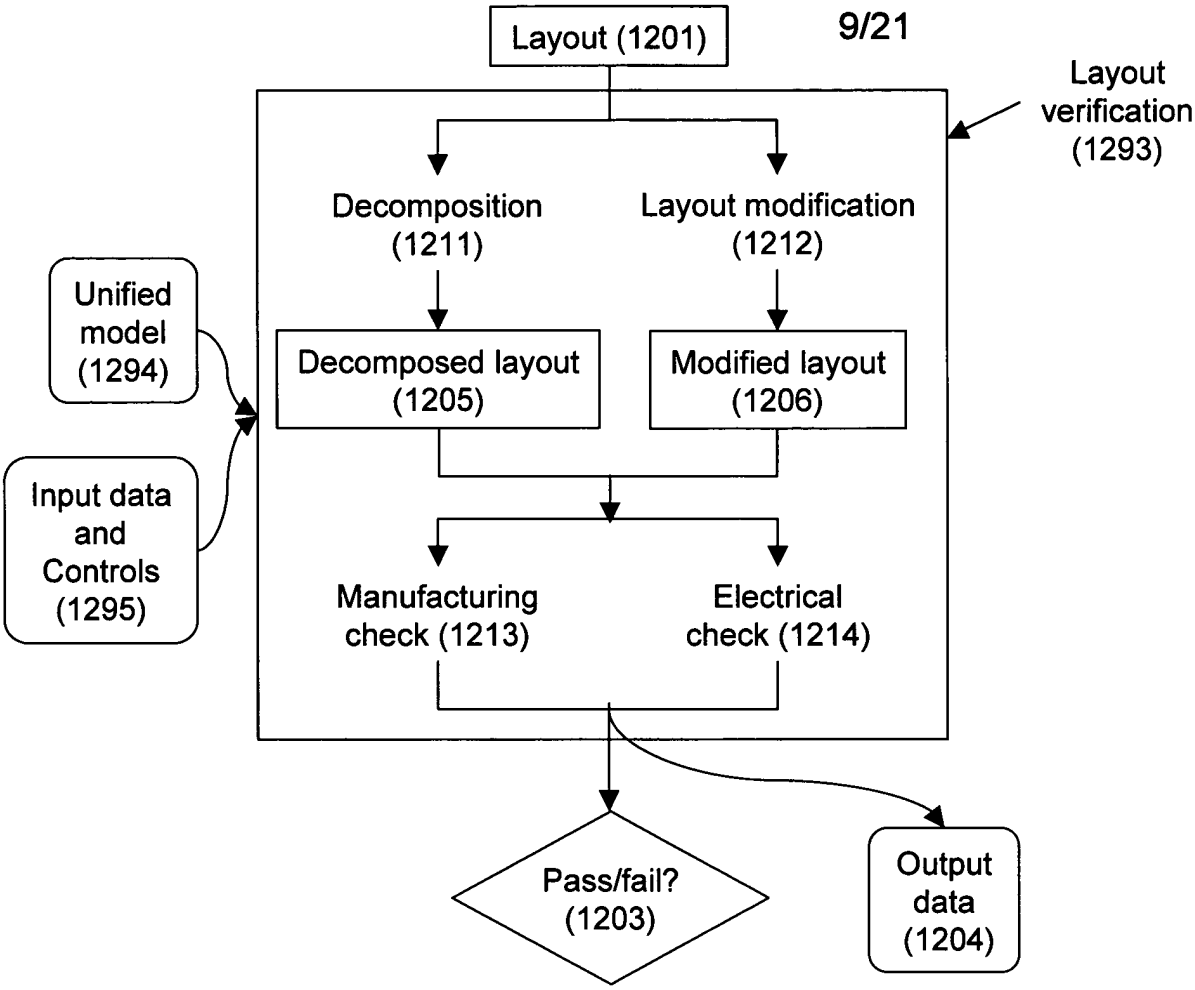

Layout (1201)
Layout verification (1293)
Decomposition (1211)
Layout modification (1212)
Unified model (1294)
Decomposed layout (1205)
Modified layout (1206)
Input data and Controls (1295)
Manufacturing check (1213)
Electrical check (1214)
Pass/fail? (1203)
Output data (1204)

Figure 12

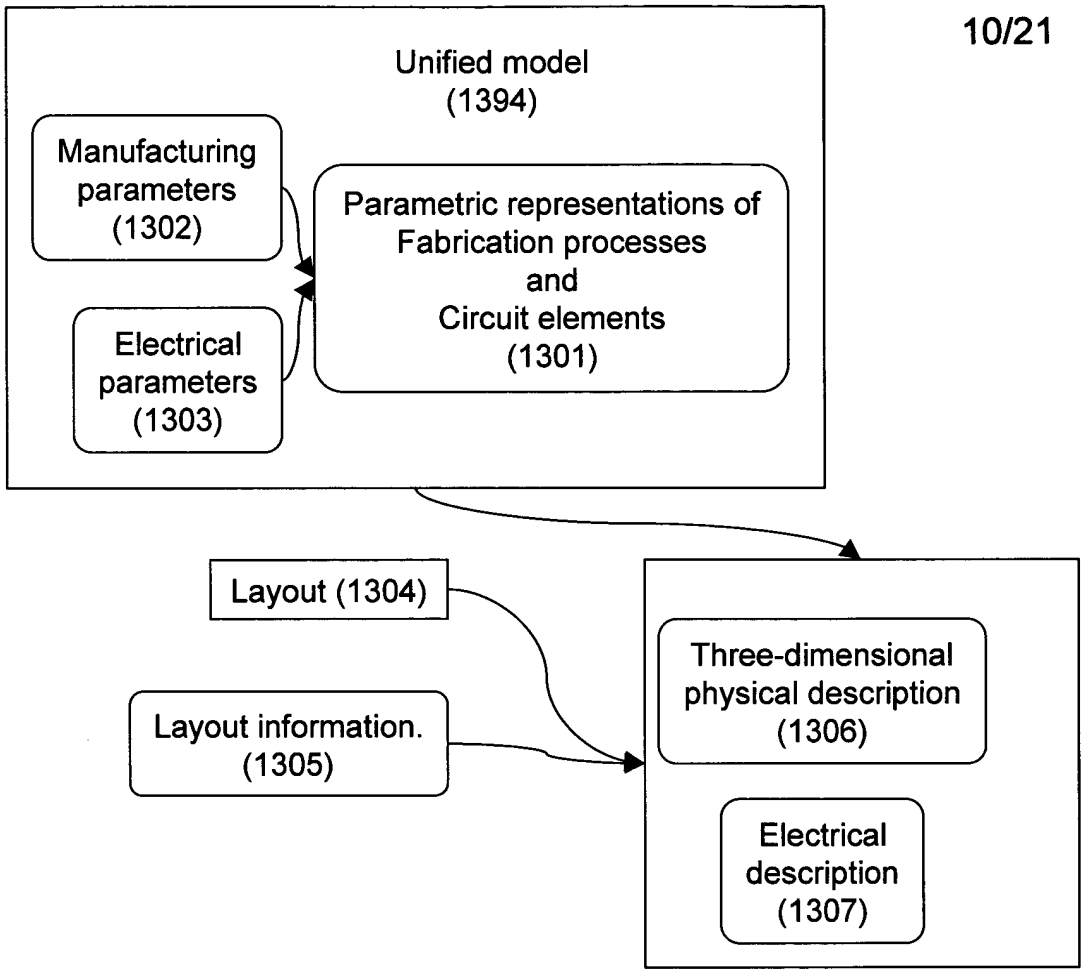
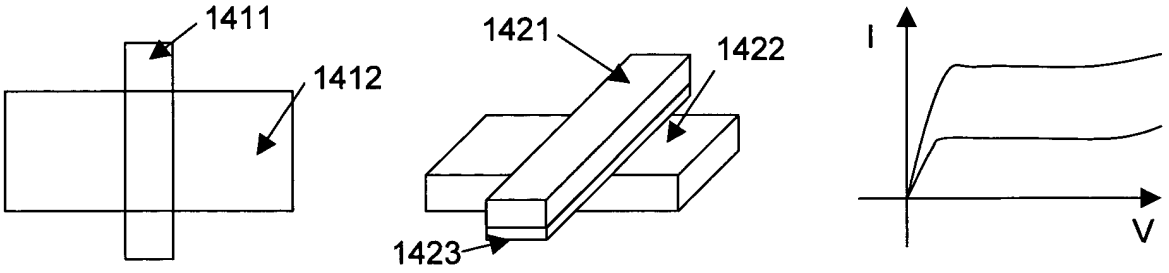


Figure 13



Layout (1401)

Three-dimensional physical description (1402)

Electrical description (1403)

Figure 14

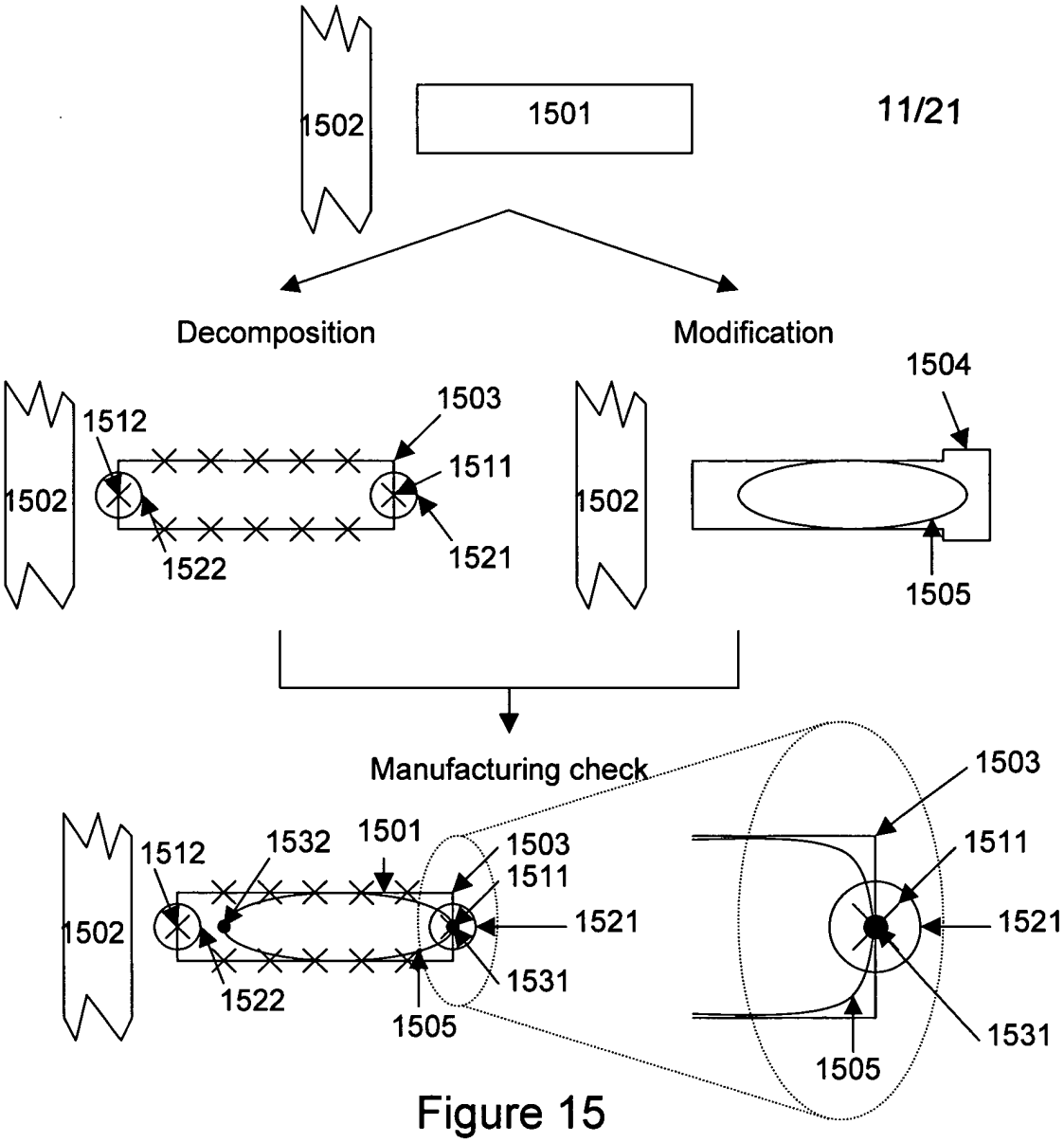


Figure 15

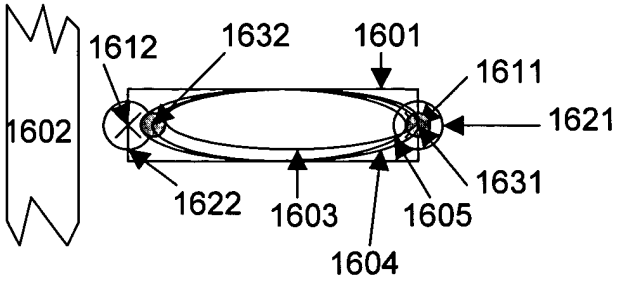


Figure 16

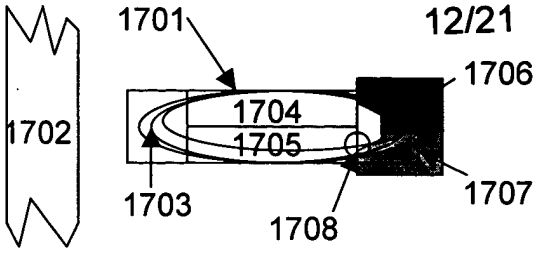


Figure 17a

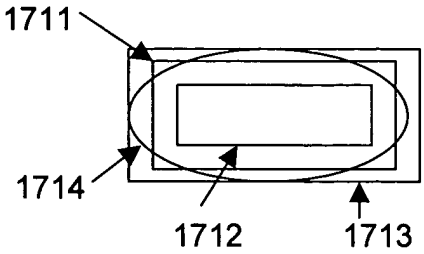
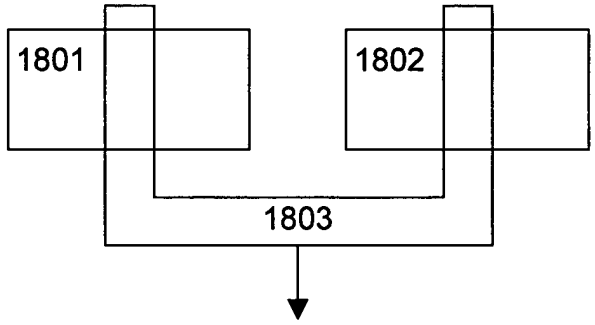


Figure 17b

Figure 18a



Decomposition

Figure 18b

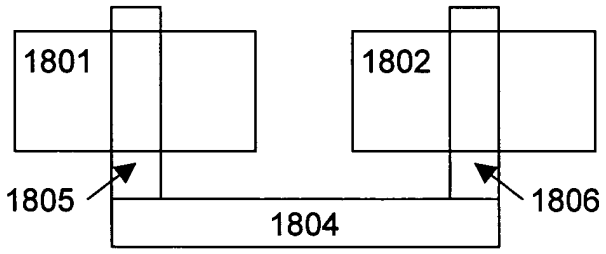
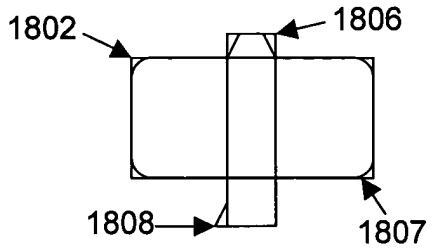


Figure 18c



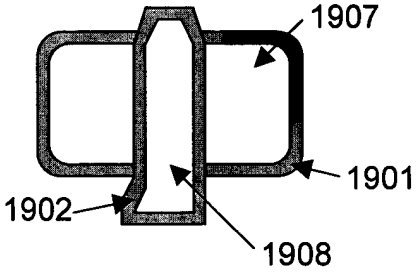


Figure 19a

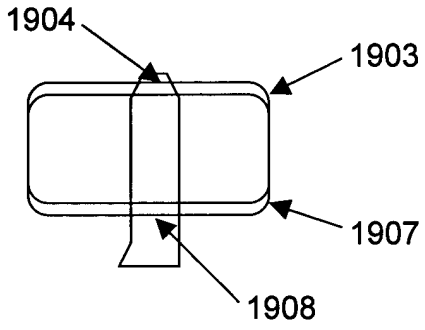


Figure 19b

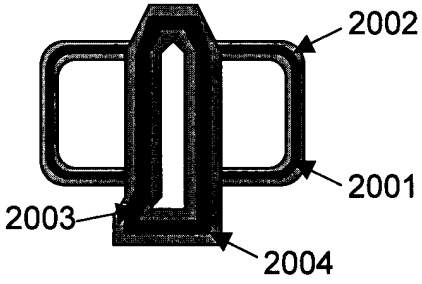


Figure 20

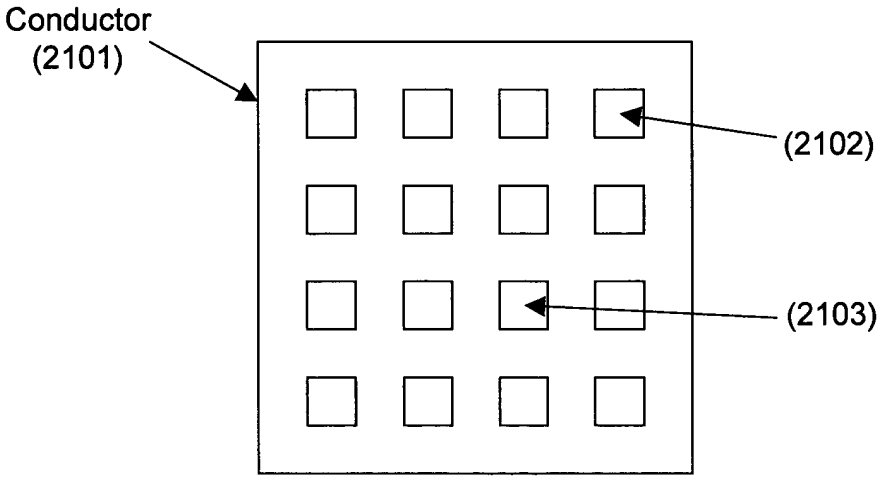


Figure 21

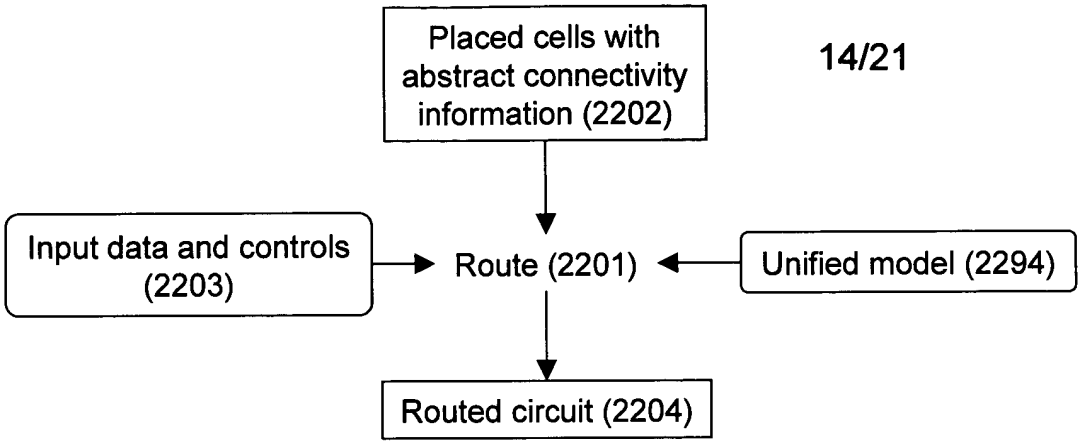

Placed cells with abstract connectivity information (2202)
Input data and controls (2203)
Route (2201)
Unified model (2294)
Routed circuit (2204)

Figure 22

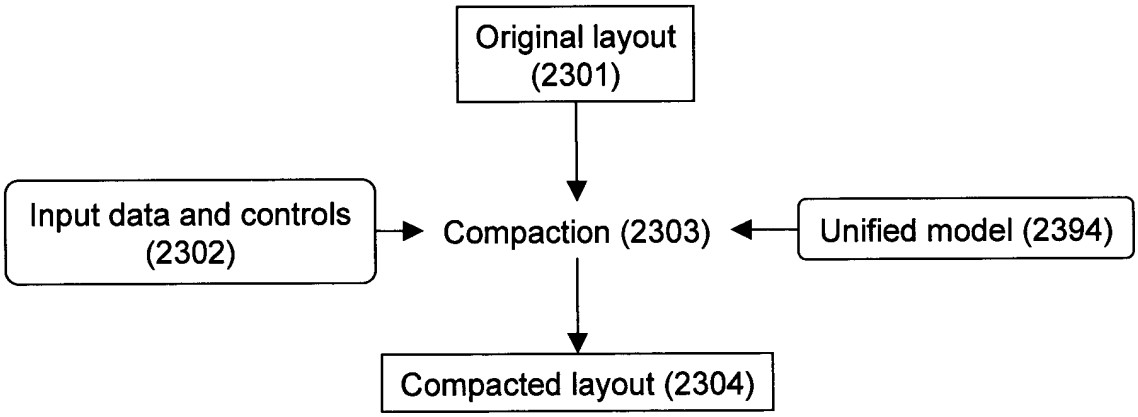


Figure 23

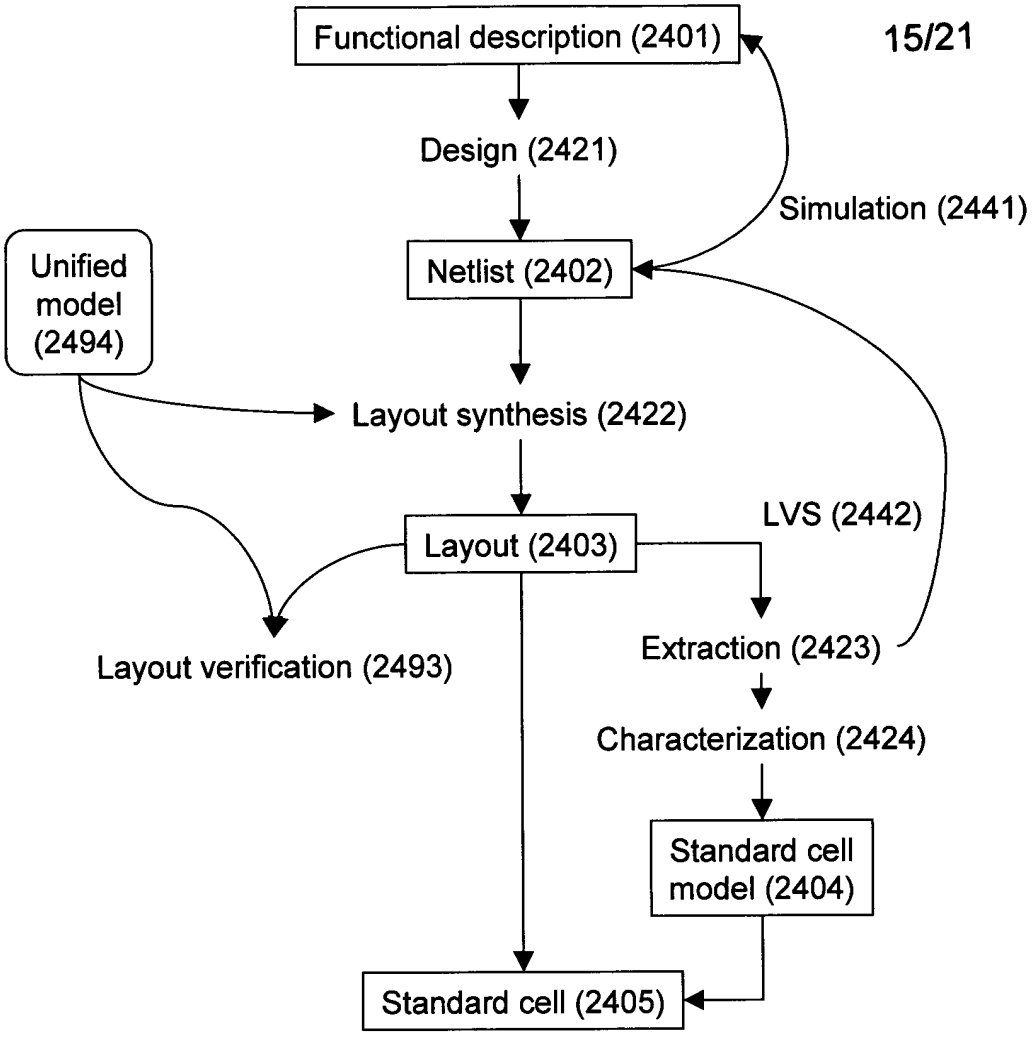


Figure 24

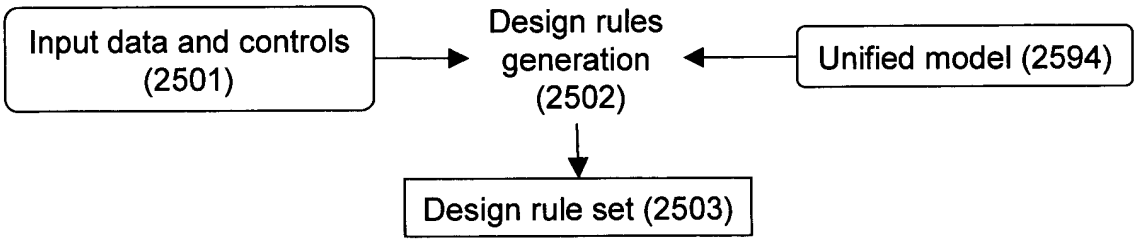


Figure 25

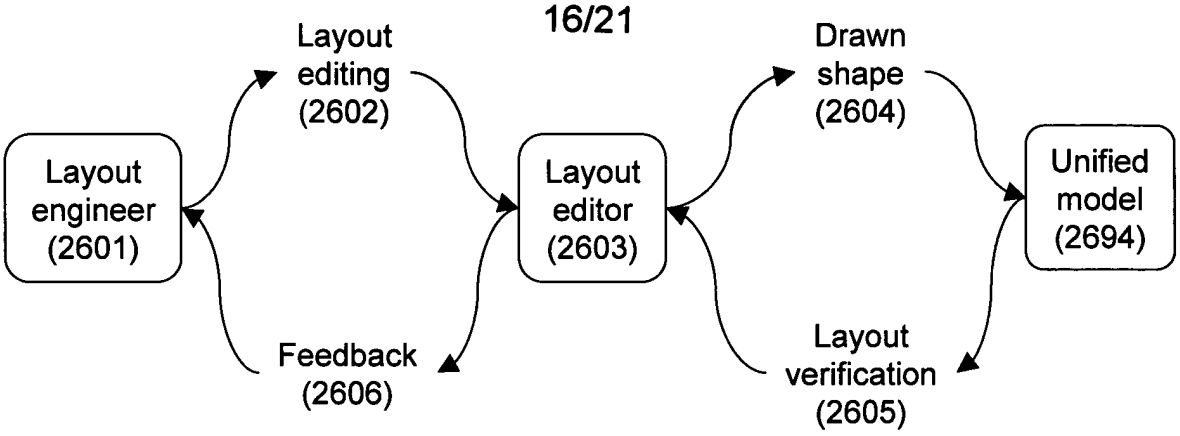


Figure 26

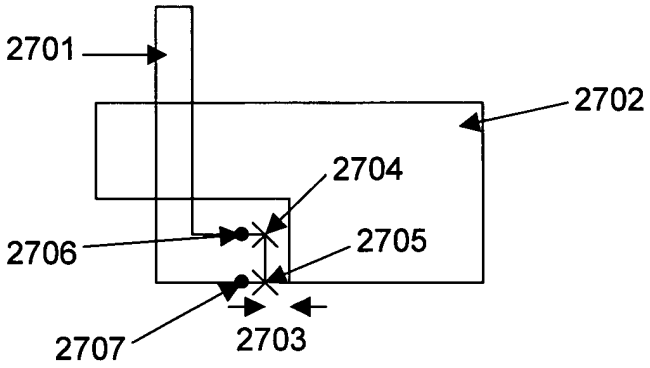


Figure 27

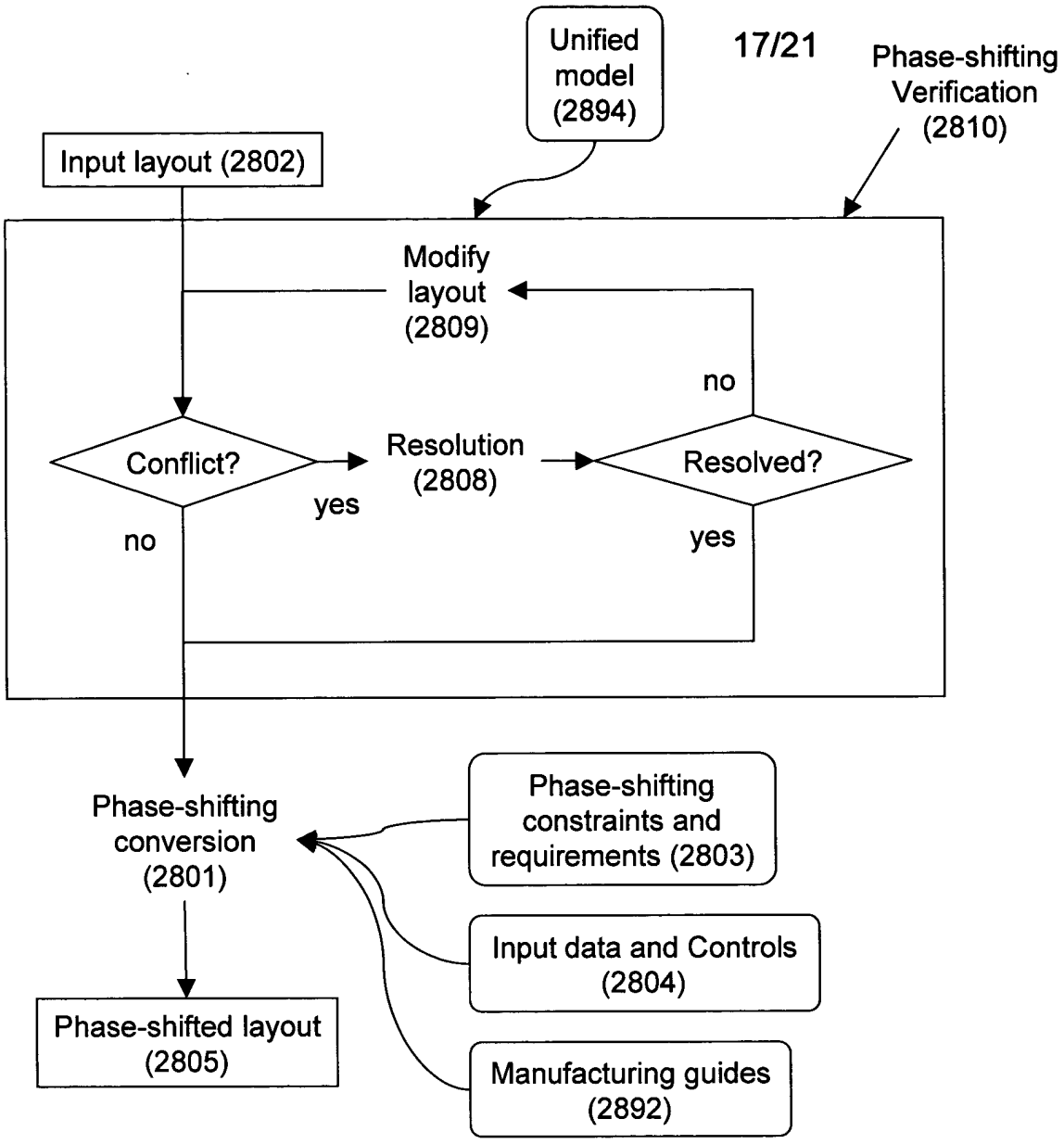

Unified model (2894)
Phase-shifting Verification (2810)
Input layout (2802)
Modify layout (2809)
no
Conflict?
Resolution (2808)
Resolved?
yes
no
yes
Phase-shifting conversion (2801)
Phase-shifting constraints and requirements (2803)
Input data and Controls (2804)
Phase-shifted layout (2805)
Manufacturing guides (2892)

Figure 28

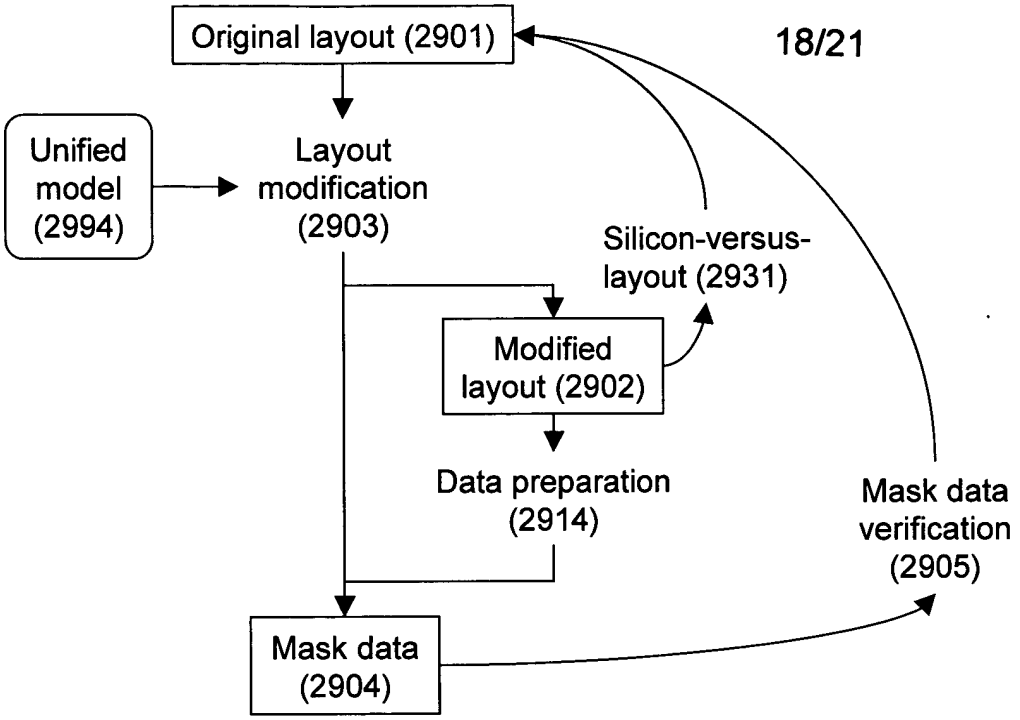


Figure 29

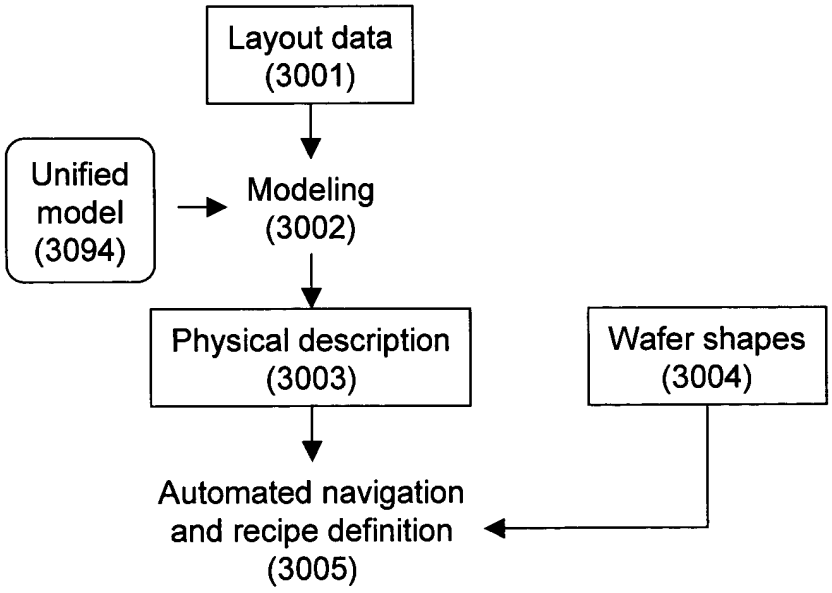


Figure 30

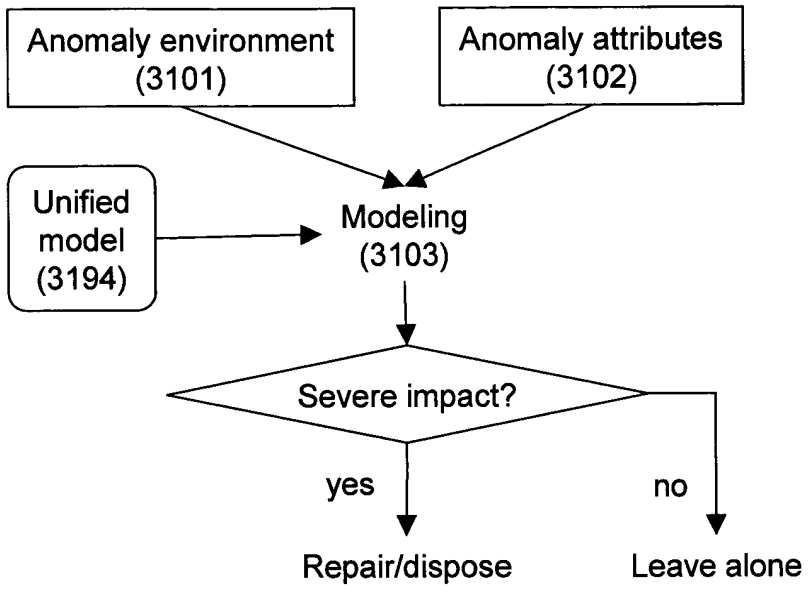


Figure 31

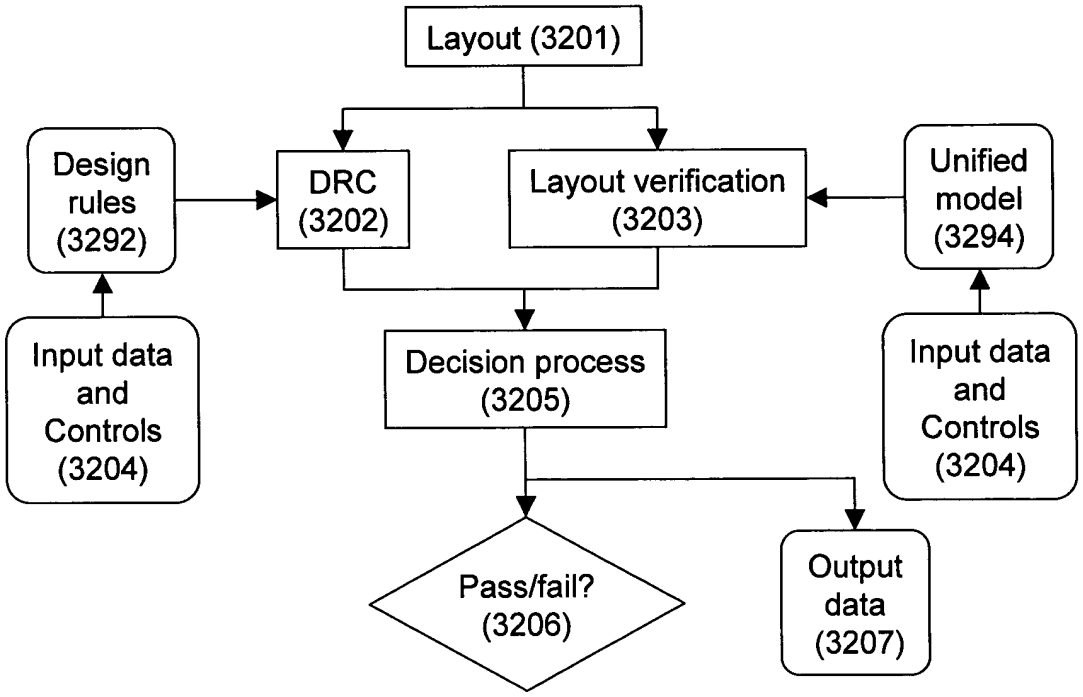


Figure 32

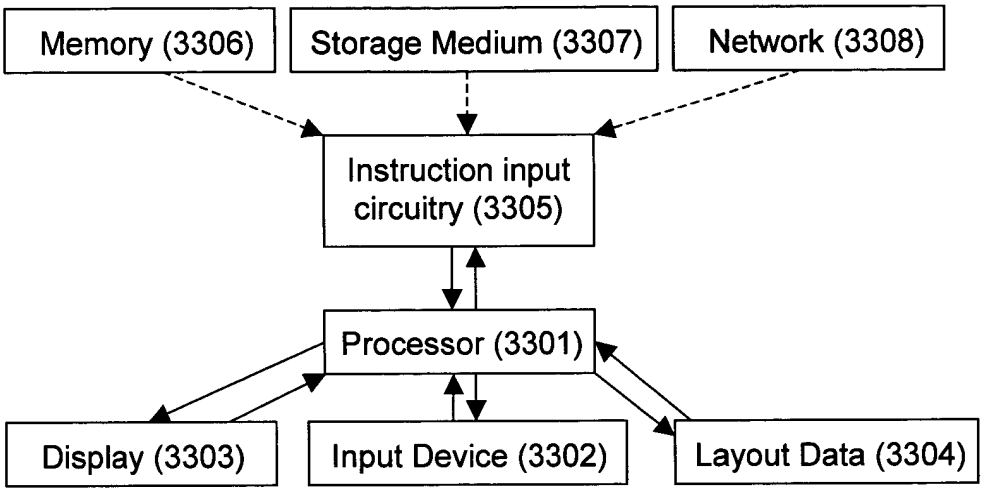


Figure 33

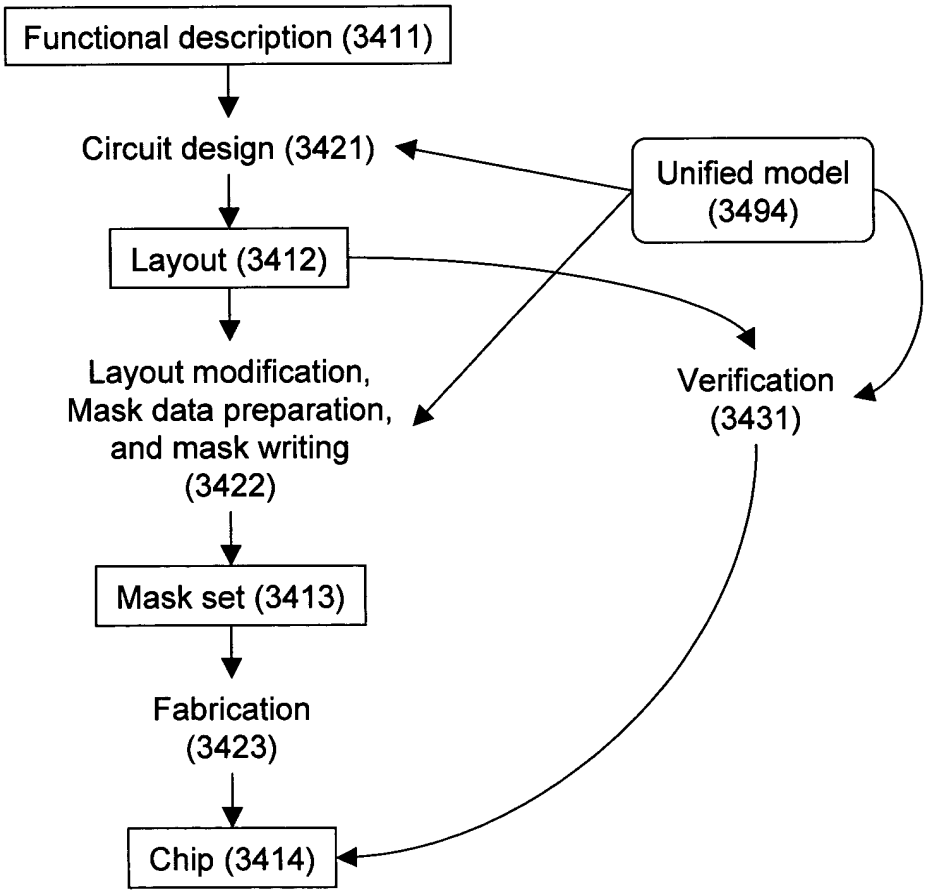


Figure 34

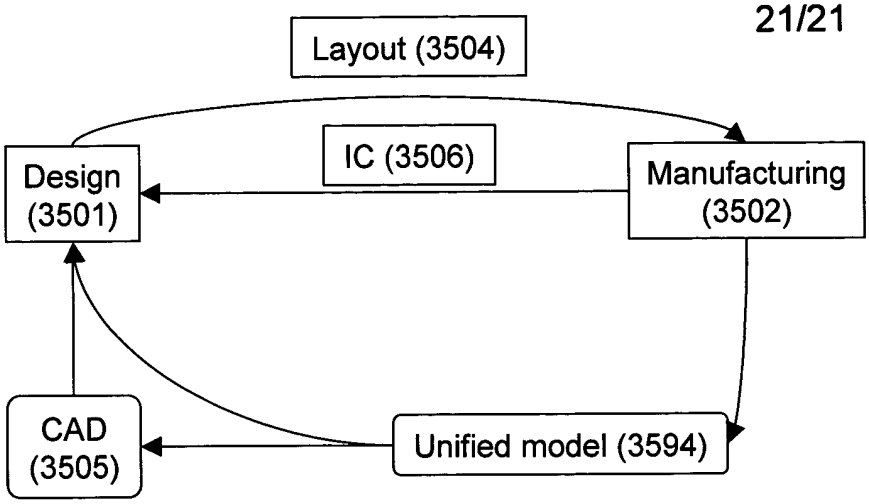


Figure 35

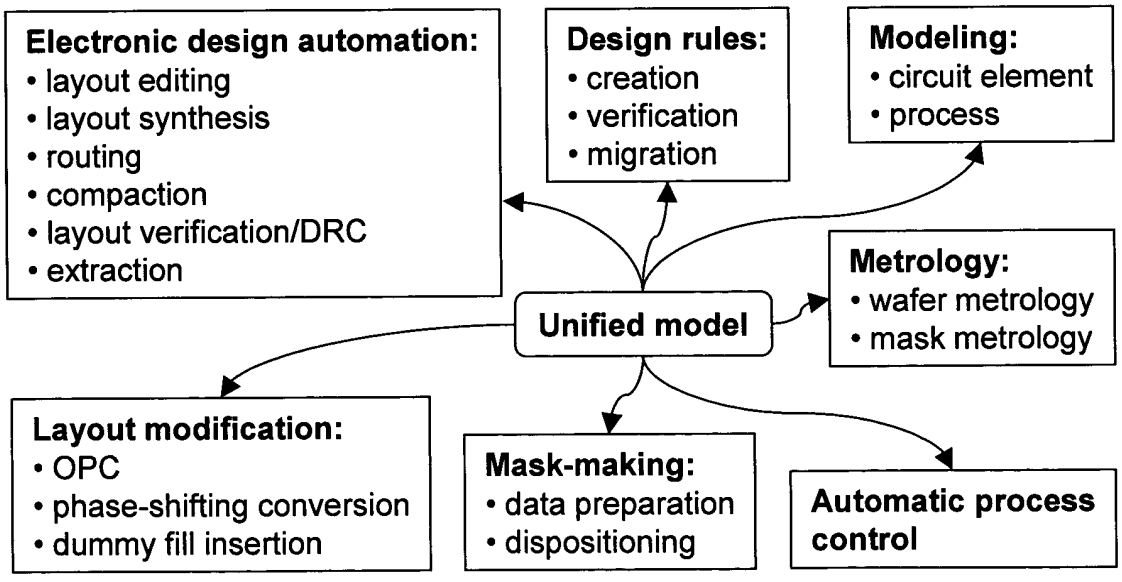


Figure 36